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09/692,852	10/20/2000	Andrew R. Osborn	65,135-008	6250

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EXAMINER	
STRANGE, AARON N	

ART UNIT	PAPER NUMBER
2153	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,852	OSBORN ET AL.	
	Examiner	Art Unit	
	Aaron Strange	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12 and 14-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 14-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06162005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Cancellation of claims 11, 13, and 48-67 is noted. Claims 1-10, 12, and 14-47 remain pending and are presented for further examination.

Response to Arguments

2. Applicant's arguments filed 6/16/2005 have been fully considered but they are not persuasive.

3. With regard to claim 7, it should be noted that claim 7 was inadvertently omitted from the prior Office action due to typographical error, and should not be interpreted as being in condition for allowance as asserted by Applicant (Page 35, Lines 8-9 of Remarks). Claim 7 contains substantially identical subject matter to claims 38-40 and is rejected under the same rationale.

4. With regard to claim 1, and Applicant's assertion that Antonov fails to disclose that the processed information is sent from the first processor toward the hub "without storing the processed information in the first real memory location of the first node" (Page 35, Lines 17-22 of Remarks), the Examiner respectfully disagrees.

Applicant cites several sections of Antonov as allegedly providing evidence supporting the above assertion (Page 36, Lines 6-19 of Remarks). However, the sections of Antonov cited by Applicant relate only to the storage of data within the

system, and was not cited in the rejection of claim 1. The "processed information" claimed in claim 1 is anticipated by the messages sent between workstations in the system disclosed by Antonov. These messages are dynamically created and sent toward the hub from the various workstations without being stored in the first real memory of the workstation. They are subsequently stored in the memory of the receiving stations since they are analyzed and may instruct the receiving station to perform particular tasks.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5,6,8,19-22,27,36,37, and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Antonov (US 5,884,046).

7. With regard to claim 1, Antonov discloses a method of communicating across a distributed multiprocessing system having a first node with a first processor and a first real memory location and a second node with a second processor and a second real memory(workstations) (Fig 2, 13), the first and second nodes are connected to a central

signal routing hub (Fig 1, 17) by first and second communication links, respectively, said method comprising the steps of:

processing information within the first processor of the first node (generate message);

addressing the processed information using at least one of the destination addresses (specify recipient);

transmitting the processed information from the first processor of the first node across the first communication link toward the hub without storing the processed information in the first real memory location of the first node (packet is generated and sent) (Col 5, Lines 49-53), thereby defining a sending node (Col 5, Lines 49-53);

receiving the processed information along with the destination address within the hub (Col 5, Lines 54-55);

identifying the destination address for the transmitted processed information within the hub;

sending the processed information without modification from the hub over at least one of the communication links to at least one of the first and second nodes associated with the destination address, thereby defining at least one addressed node (inter-workstation message is received and routed to recipient) (Col 5, Lines 55-65);

and storing the processed information within the real memory location of the addressed node (messages are stored and may be executed if they are store /retrieve requests) (Col 5, Line 60 to Col 6, Line 51).

Antonov fails to specifically recite indexing the first and second nodes to

define different destination addresses for each of the nodes. However, in order for the processors to communicate with each other, they must be assigned a destination address in order for messages to be properly routed. Therefore, Antonov further discloses indexing the fist and second nodes to define different destination addresses for each of the nodes, since the nodes are able to identify and communicate with other nodes (Col 5, Lines 49-51).

8. With regard to claim 2, Antonov further discloses that the step of processing information is further defined as creating data (creating a message) within the first processor (Col 5, Lines 49-53).

9. With regard to claim 3, Antonov further discloses that the step of processing information is further defined as compiling the data (creating a packet with the message and addressing information) within the first processor (Col 5, Lines 49-53).

10. With regard to claim 5, Antonov further discloses that the step of transmitting the processed information is further defined as transmitting the processed information across the first communication link in only one direction from the first processor to the hub to define a send-only system (The packet is sent directly to the hub) (Col 5, Lines 49-55 and Fig 2).

11. With regard to claim 6, Antonov further discloses that the step of sending the processed information without modification is further defined as sending the processed information from the hub over at least one of the communication links in only one direction from the hub to at least one of the first and second nodes to the hub to further define the send-only system (The packet is forwarded to the recipient by the hub) (Col 5, Lines 54-65).

12. With regard to claim 8, as discussed regarding claim 1, Antonov fails to specifically recite indexing the first and second processors to define a different code for each of the processors for differentiating the processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses indexing the fist and second nodes to define an identifierfor each of the nodes for differentiating the nodes, since the nodes are able to identify and communicate with other nodes (Col 5, Lines 49-51).

13. With regard to claim 19, Antonov discloses a distributed multiprocessing system comprising:

a first node and a second node with said nodes being separated from each other (workstations) (Fig 2, 13),

a first processor disposed within said first node for processing information and for assigning a first address to a first processed information (workstations contain processors),

a first real memory location disposed within said first node for storing processed information at said first node (workstations contain memory);

a second processor disposed within said second node for processing information and for assigning a second address to a second processed information (workstation) (Fig 2, 13), a central signal routing hub (Fig 1, 17),

a second real memory location disposed within said second node for storing processed information at said second node (workstations contain memory),

a first communication link interconnecting said first node and said hub for transmitting said first processed information between said first processor of said first node and said hub without storing said processed information within said first real memory location of said first node, (Fig 2, 11C);

a second communication link interconnecting said second node and said hub for transmitting said second processed information between said second processor of said second node and said hub without storing said processed information within said second real memory location of said second node, (Fig 2, 11),

said central routing hub including a sorter for receiving at least one of said first and second processed information from at least one of said first and second nodes, thereby defining at least one sending node (Message is received at a processing node) (Col 5, Lines 54-55), and for associating a destination of at least one of said first and

second addresses of said first and second processed information, respectively, with at least one of said destination addresses, and for sending at least one of said first and second processed information without modification from said hub over at least one of said communication link to at least one of said first and second nodes associated with said destination address, thereby defining at least one addressed node (message is routed to the recipient) (Col 5, Lines 55-65), with said first and second real memory locations storing processed information received from said hub (messages are stored and may be executed if they are store /retrieve requests) (Col 5, Line 60 to Col 6, Line 51).

Antonov fails to specifically recite an indexer connected to said routing hub for indexing said first and second nodes to define different destination addresses for each of said nodes. However, in order for the processors to communicate with each other, they must be assigned a destination address in order for messages to be properly routed. Since the nodes are able to identify and communicate with other processors (Col 5, Lines 49-51), Antonov further discloses an indexer indexing the first and second nodes to define different destination addresses for each of the nodes. The indexer must be connected to the hub since the messages are routed by the hub and it must have the appropriate addresses in order to properly route the messages.

14. With regard to claims 20 and 21, Antonov further discloses that said first and second communications links each include incoming and outgoing transmission lines (Fig 1, 11 and 11C). Since the workstations can communicate in both directions in order

to request and send data to each other, incoming and outgoing transmission lines are present (Col 6, Lines 40-50).

15. With regard to claim 27, as discussed regarding claims 1 and 19, Antonov fails to specifically recite an indexer connected to said routing hub which defines a different code for each of said processors for differentiating said processors. However, in order for the processors to communicate with each other, they must be differentiated in order for messages to be routed to the intended recipient. Therefore, Antonov further discloses that the indexer defines an identifier for each of said nodes for differentiating said nodes, since the nodes are able to identify and communicate with other nodes (Col 5, Lines 49-51).

16. With regard to claims 36 and 37, Antonov further discloses that each of first and second processors include at least one task and executable code for processing information defined by each of said tasks (Col 5, Line 46 to Col 6, Line 51). The first and second processors generate and receive messages as well as respond to them with any data that may have been requested. Executable instructions are necessary for the processors to perform these tasks.

17. With regard to claim 47, Antonov further discloses that said sorter includes hardware for determining destination addresses of said addressed nodes (Col 6, Lines 8-16).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 14-17, 33-35, 41,42, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046).

20. With regard to claims 14-17, and 33-35, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose connecting an additional hub, having third and fourth nodes, by a hub link and reconfiguring the system so that the third and fourth nodes may communicate with the first and second nodes.

However, Antonov discloses that the invention should be scalable to allow for the addition of mode nodes, and further states that the type of interconnect is not limited to any specific type (Col 4, Lines 32-33). Connecting another hub with additional processors and reconfiguring the system to notify the newly connected processors and the current processors about each other would have been an advantageous way to scale the system since it would have allowed additional processors to be added to the system and communicate with the processors already present, and would have allowed independent implementations of the invention to be combined into a single network.

This would allow the system to be easily scaled by connecting additional hubs as needed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect another hub with additional processors and reconfigure the system to notify the newly connected processors and the current processors about each other. This would have allowed the system to be scaled by adding additional hubs and processors as needed.

21. With regard to claims 41 and 42, Antonov further discloses a chipset interconnected between each of said incoming and outgoing communication links and said corresponding processors for creating a virtually transparent connection there between and a buffer disposed between each of said processors and said chipsets. Antonov discloses that workstations are connected to the processing nodes via network links (Col 5, Lines 6-7). All network links require a chipset that prepares packets for transmission over them, as well as a buffer for holding data prior to packaging the data into a packet for transmission.

22. With regard to claims 45 and 46, the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), including a host computer connected to one of said first and second nodes, having a processing card. All of the workstations disclosed by Antonov are host computers connected to their respective processor and connected to the processing nodes of the central hub via a

network link (Col 5, Lines 6-7). The workstations disclosed by Antonov must have a processing card since they communicate via a network, which requires a network card capable of processing signals to access. Antonov fails to specifically disclose said host computer having a processing card and at least one peripheral device.

The Examiner takes Official Notice that peripheral devices such as monitors and keyboards are old and well known in the art and are components of virtually every workstation computer. These devices are well known and advantageous since they allow users to interact with a workstation using a monitor and keyboard.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made provide peripherals such as a monitor and keyboard to allow users to interact with the workstations in the system disclosed by Antonov.

23. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Kisor (US 6,098,091).

24. With regard to claim 4, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose that the step of transmitting the processed information is further defined as transmitting data along with executable code from the sending node to the addressed node.

Kisor discloses a sytem where a computer can assign tasks to idle remote computers, which can work on the task and return completed results. This allows the results to be calculated much faster since a plurality of computers can work on the data

in parallel. Kisor discloses that data and instructions for competing the assigned task are sent to the remote computer when the task is assigned (Col 6, Lines 31-35). This would have been an advantageous addition to the system disclosed by Antonov since it would have allowed workstations to assign tasks to other workstations by sending data and executable instructions to them. This would have allowed calculations to be performed much more quickly.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow transmission of data along with executable instructions between the processors since it would have allowed one processor to work on data for another processor to speed up the completion of a task.

25. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Spurgeon.

26. The Examiner would like to note that the Spurgeon reference is an excerpt from a book, obtained through Safari Tech Books Online. Only the relevant cited sections have been included with the Office action, since the entire reference is several hundred pages.

27. With regard to claims 22-24, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose that the incoming and outgoing transmission lines transmit signals in only one direction, defining a send-only system or that the links are unidirectional fiber. Antonov

does disclose that the workstations communicate with the hub via a Local Area Network (Col 5, Lines 46-49).

Spurgeon discloses the use of unidirectional fiber optic cables for implementing an Ethernet network. Ethernet is a well-known and very common type of Local Area Network. The 10BASE-FL standard for Ethernet requires the use of two unidirectional fiber links for transmitting and receiving data. Optical fibers are advantageous since they are completely electrically isolated, and are immune to electrical interference (Spurgeon, Section 8.3.1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use unidirectional fiber links for the incoming and outgoing transmission lines to define a send only system. This would have allowed full duplex communication across electrically isolated connections, allowing the system to be used in areas with large amounts of electrical noise, such as a manufacturing environment.

28. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Eidson (US 6,125,420).

29. With regard to claims 25 and 26, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose at least one actuator connected to at least one of said first and second node,

respectively, for performing a testing operation during an operation of said system or that said actuator is a servo-hydraulic actuator.

Eidson discloses the use of actuators in a distributed control system to implement control functions for controlling devices connected to the system (Col 4, Lines 56-67). Servo-hydraulic actuators are a well-known type of actuator, and it would have been a matter of preference to the system designer to choose that particular type of actuator. These would have been an advantageous addition to the system disclosed by Antonov since it would have allowed the workstations to send data and instructions to processors connected to actuators to control devices connected to the system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect actuators to at least one processor to allow instructions to be sent to that processor to control devices connected to the system through the actuator.

30. Claims 18, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Grohn et al. (US 6,405,337).

31. With regard to claims 18, 43 and 44, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose including a counter for determining a number of times said processed information is sent to said addressed node, a sequencer for monitoring and

controlling a testing operation as performed by said system, or limiting the number of times that said processed information can be sent from a sending node.

Grohn teaches the use of a retransmission counter to count the number of times processed information is sent to a processor. Grohn further discloses a sequencer for monitoring and controlling a testing operation as performed by said system (current delays are compared to retransmission timeout) (Col 6, Line 62 to Col 7, Line 7). The current delays are compared with the retransmission timeout to determine when to decrement the counter. When the counter reaches zero, the communication line is assumed to have failed (Col 6, Lines 28-30 and Col 7, Lines 3-7). This causes the sending station to stop attempting retransmissions and allows error handling procedures to start.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a counter to count the number of times said processed information is sent to said addressed processor and use a sequencer for monitoring and controlling a testing operation as performed by said system. This would have allowed error handling procedures to begin and stop the sending processor from attempting further retransmissions.

32. Claims 7 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Hillis (US 5,978,570).

33. With regard to claims 7 and 38-40, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), it fails to specifically disclose the use of pointers for directing the flow of data between nodes or directing a processor to a subsequent task to be performed.

Hillis teaches the use of pointers to direct a processor to a subsequent task to be performed and directing the flow of data between processors. Hillis discloses a task register holding a pointer to the next task and a next register holding a pointer to the next virtual processor in the list of virtual processors on the task (Col 14, Lines 65-67). The pointer is advanced through the list until an order has been executed for all processors in the list for that task (Col 14, Lines 24-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use pointers for directing the flow of data between processors or directing a processor to a subsequent task to be performed since they allow a linked list of items in memory to be quickly traversed and executed.

34. Claims 9-13 and 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonov (US 5,884,046) in view of Blumrich et al.

35. With regard to claims 9 and 28, while the system disclosed by Antonov shows substantial features of the claimed invention (discussed above), including that the first and second node can address and forward processed information to each of the indexed processors within the system, it fails to specifically disclose creating a virtual

memory map of each of the identifiers within each of the first and second processors for this purpose.

Blumrich teaches the use of virtual memory maps to map virtual memory locations to nodes in a distributed system. This allows messages to be sent to other nodes simply by addressing them to the virtual memory location, reducing overhead required to transfer data (Page 2, Section 2 and Page 6, Section 4.2). This would have been an advantageous addition to the system disclosed by Antonov since it greatly reduces the overhead of communication between nodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a virtual memory map as disclosed by Blumrich to contain addressing information for each of the processors in the system. This would have greatly reduces the overhead required for sending messages between the nodes in the system.

36. With regard to claims 10 and 30, Antonov further discloses that addressing the processed information is further defined as assigning a destination address onto the processed information indicative of the code of the addressed processor (Packets identify the workstation they are intended for) (Col 5, Lines 49-53).

37. With regard to claim 31, Antonov further discloses that said first real memory location is connected to said hardware portion of said first processor and said second real memory location is connected to said hardware portion of said second processor.

The memory and processors within workstations are connected to each other, since they must be able to interact in order to operate properly.

38. With regard to claims 12 and 32, as discussed regarding claims 10 and 30, Antonov further discloses that addressing the processed information is further defined as assigning a memory address onto the processed information corresponding to a location of the real memory location of the addressed node (Packets identify the workstation they are intended for) (Col 5, Lines 49-53).

39. With regard to claim 29, Antonov further discloses that each of said first and second processors further include a hardware portion for assigning said first and second addresses to said first and second processed information, respectively. Antonov discloses that the workstations generate a data packet identifying another workstation to send the message to (Col 5, Lines 49-53). In order to generate the data packet identifying another workstation a hardware portion must be present in order to assign the correct address to the data and generate the packet.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

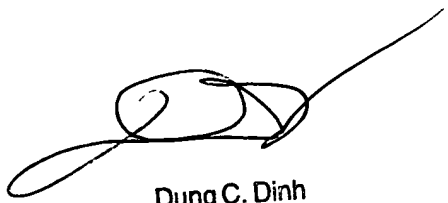
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

41. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron Strange whose telephone number is 571-272-3959. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Dung C. Dinh
Primary Examiner

AS 8/26/2005